EXHIBIT 6
FILED UNDER SEAL

Exhibit
0001

DDR4 SDRAM

MT40A2G4
MT40A1G8
MT40A512M16

Features

- $V_{DD} = V_{DDQ}$ = 1.2V ±60mV
- V_{PP} = 2.5V, –125mV, +250mV
- On-die, internal, adjustable V_{REFDQ} generation
- 1.2V pseudo open-drain I/O
- Refresh time of 8192-cycle at T_C temperature range:
  - 64ms at -40°C to 85°C
  - 32ms at >85°C to 95°C
  - 16ms at >95°C to 105°C
- 16 internal banks (x4, x8): 4 groups of 4 banks each
- 8 internal banks (x16): 2 groups of 4 banks each
- 8*n*-bit prefetch architecture
- Programmable data strobe preambles
- Data strobe preamble training
- Command/Address latency (CAL)
- Multipurpose register READ and WRITE capability
- Write leveling
- Self refresh mode
- Low-power auto self refresh (LPASR)
- Temperature controlled refresh (TCR)
- Fine granularity refresh
- Self refresh abort
- Maximum power saving
- Output driver calibration
- Nominal, park, and dynamic on-die termination (ODT)
- Data bus inversion (DBI) for data bus
- Command/Address (CA) parity
- Databus write cyclic redundancy check (CRC)
- Per-DRAM addressability
- Connectivity test
- JEDEC JESD-79-4 compliant
- sPPR and hPPR capability
- MBIST-PPR support (Die Revision R only)

Options[1]	Marking
• Configuration	
– 2 Gig x 4	2G4
– 1 Gig x 8	1G8
– 512 Meg x 16	512M16
• 78-ball FBGA package (Pb-free) – x4, x8	
– 9mm x 13.2mm – Rev. A	PM
– 8mm x 12mm – Rev. B, D, G	WE
– 7.5mm x 11mm – Rev. E, H, J, R	SA
• 96-ball FBGA package (Pb-free) – x16	
– 9mm x 14mm – Rev. A	HA
– 8mm x 14mm – Rev. B	JY
– 7.5mm x 13.5mm – Rev. D, E, H	LY
– 7.5mm x 13mm – Rev. J, R	TB
• Timing – cycle time	
– 0.625ns @ CL = 22 (DDR4-3200)	-062E
– 0.682ns @ CL = 21 (DDR4-2933)	-068
– 0.750ns @ CL = 19 (DDR4-2666)	-075
– 0.750ns @ CL = 18 (DDR4-2666)	-075E
– 0.833ns @ CL = 17 (DDR4-2400)	-083
– 0.833ns @ CL = 16 (DDR4-2400)	-083E
– 0.937ns @ CL = 15 (DDR4-2133)	-093E
– 1.071ns @ CL = 13 (DDR4-1866)	-107E
• Operating temperature	
– Commercial (0° ≤ T_C ≤ 95°C)	None
– Industrial (–40° ≤ T_C ≤ 95°C)	IT
– Automotive (–40° ≤ T_C ≤ 105°C)	AT
• Revision	:A, :B, :D, :E, :G, :H, :J, :R

Notes: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

Table 1: Key Timing Parameters

Speed Grade[1]	Data Rate (MT/s)	Target CL-*n*RCD-*n*RP	^tAA (ns)	^tRCD (ns)	^tRP (ns)
-062Y	3200	22-22-22	13.75 (13.32)	13.75 (13.32)	13.75 (13.32)
-062E	3200	22-22-22	13.75	13.75	13.75
-068	2933	21-21-21	14.32 (13.75)	14.32 (13.75)	14.32 (13.75)
-075E	2666	18-18-18	13.50	13.50	13.50

Products and specifications discussed herein are subject to change by Micron without notice.

Table 8: Burst Type and Burst Order

Note 1 applies to the entire table

Burst Length	READ/ WRITE	Starting Column Address (A[2, 1, 0])	Burst Type = Sequential (Decimal)	Burst Type = Interleaved (Decimal)	Notes
BC4	READ	0 0 0	0, 1, 2, 3, T, T, T, T	0, 1, 2, 3, T, T, T, T	2, 3
		0 0 1	1, 2, 3, 0, T, T, T, T	1, 0, 3, 2, T, T, T, T	2, 3
		0 1 0	2, 3, 0, 1, T, T, T, T	2, 3, 0, 1, T, T, T, T	2, 3
		0 1 1	3, 0, 1, 2, T, T, T, T	3, 2, 1, 0, T, T, T, T	2, 3
		1 0 0	4, 5, 6, 7, T, T, T, T	4, 5, 6, 7, T, T, T, T	2, 3
		1 0 1	5, 6, 7, 4, T, T, T, T	5, 4, 7, 6, T, T, T, T	2, 3
		1 1 0	6, 7, 4, 5, T, T, T, T	6, 7, 4, 5, T, T, T, T	2, 3
		1 1 1	7, 4, 5, 6, T, T, T, T	7, 6, 5, 4, T, T, T, T	2, 3
	WRITE	0, V, V	0, 1, 2, 3, X, X, X, X	0, 1, 2, 3, X, X, X, X	2, 3
		1, V, V	4, 5, 6, 7, X, X, X, X	4, 5, 6, 7, X, X, X, X	2, 3
BL8	READ	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	
		0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6	
		0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5	
		0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4	
		1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3	
		1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2	
		1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1	
		1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0	
	WRITE	V, V, V	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	3

Notes: 1. 0...7 bit number is the value of CA[2:0] that causes this bit to be the first read during a burst.
2. When setting burst length to BC4 (fixed) in MR0, the internal WRITE operation starts two clock cycles earlier than for the BL8 mode, meaning the starting point for ^{t}WR and ^{t}WTR will be pulled in by two clocks. When setting burst length to OTF in MR0, the internal WRITE operation starts at the same time as a BL8 (even if BC4 was selected during column time using A12/BC4_n) meaning that if the OTF MR0 setting is used, the starting point for ^{t}WR and ^{t}WTR will not be pulled in by two clocks as described in the BC4 (fixed) case.
3. T = Output driver for data and strobes are in High-Z.
V = Valid logic level (0 or 1), but respective buffer input ignores level on input pins.
X = "Don't Care."

CAS Latency

The CAS latency (CL) setting is defined in the MR0 Register Definition table. CAS latency is the delay, in clock cycles, between the internal READ command and the availability of the first bit of output data. The device does not support half-clock latencies. The overall read latency (RL) is defined as additive latency (AL) + CAS latency (CL): RL = AL + CL.

Output Driver Impedance Control

The output driver impedance of the device is selected by MR1[2,1], as shown in the MR1 Register Definition table.

ODT $R_{TT(NOM)}$ Values

The device is capable of providing three different termination values: $R_{TT(Park)}$, $R_{TT(NOM)}$, and $R_{TT(WR)}$. The nominal termination value, $R_{TT(NOM)}$, is programmed in MR1. A separate value, $R_{TT(WR)}$, may be programmed in MR2 to enable a unique R_{TT} value when ODT is enabled during WRITE operations. The $R_{TT(WR)}$ value can be applied during WRITE commands even when $R_{TT(NOM)}$ is disabled. A third R_{TT} value, $R_{TT(Park)}$, is programed in MR5. $R_{TT(Park)}$ provides a termination value when the ODT signal is LOW.

Additive Latency

The ADDITIVE LATENCY (AL) operation is supported to make command and data buses efficient for sustainable bandwidths in the device. In this operation, the device allows a READ or WRITE command (either with or without auto precharge) to be issued immediately after the ACTIVATE command. The command is held for the time of AL before it is issued inside the device. READ latency (RL) is controlled by the sum of the AL and CAS latency (CL) register settings. WRITE latency (WL) is controlled by the sum of the AL and CAS WRITE latency (CWL) register settings.

Table 11: Additive Latency (AL) Settings

A4	A3	AL
0	0	0 (AL disabled)
0	1	CL - 1
1	0	CL - 2
1	1	Reserved

Notes: 1. AL has a value of CL - 1 or CL - 2 based on the CL values programmed in the MR0 register.

Rx CTLE Control

The Mode Register for Rx CTLE Control MR1[A13,A6,A5] is vendor specific. Since CTLE circuits can not be typically bypassed a disable option is not provided. Instead, a vendor optimized setting is given. It should be noted that the settings are not specifically linear in relationship to the vendor optimized setting, so the host may opt to instead walk through all the provided options and use the setting that works best in their environment.

Write Leveling

For better signal integrity, the device uses fly-by topology for the commands, addresses, control signals, and clocks. Fly-by topology benefits from a reduced number of stubs and their lengths, but it causes flight-time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the controller to maintain ^{t}DQSS, ^{t}DSS, and ^{t}DSH specifications. Therefore, the device supports a write leveling feature that allows the controller to compensate for skew.

Output Disable

The device outputs may be enabled/disabled by MR1[12] as shown in the MR1 Register Definition table. When MR1[12] is enabled (MR1[12] = 1) all output pins (such as DQ and DQS) are disconnected

Table 14: MR2 Register Definition (Continued)

Mode Register	Description
7:6	**Low-power auto self refresh (LPASR) – Mode summary** 00 = Manual mode - Normal operating temperature range (T_C: -40°C–85°C) 01 = Manual mode - Reduced operating temperature range (T_C: -40°C–45°C) 10 = Manual mode - Extended operating temperature range (T_C: -40°C–105°C) 11 = ASR mode - Automatically switching among all modes
5:3	**CAS WRITE latency (CWL) – Delay in clock cycles from the internal WRITE command to first data-in 1tCK WRITE preamble** 000 = 9 (DDR4-1600)[1] 001 = 10 (DDR4-1866) 010 = 11 (DDR4-2133/1600)[1] 011 = 12 (DDR4-2400/1866) 100 = 14 (DDR4-2666/2133) 101 = 16 (DDR4-2933,3200/2400) 110 = 18 (DDR4-2666) 111 = 20 (DDR4-2933, 3200)
	CAS WRITE latency (CWL) – Delay in clock cycles from the internal WRITE command to first data-in 2tCK WRITE preamble 000 = N/A 001 = N/A 010 = N/A 011 = N/A 100 = 14 (DDR4-2400) 101 = 16 (DDR4-2666/2400) 110 = 18 (DDR4-2933, 3200/2666) 111 = 20 (DDR4-2933, 3200)
8, 2	**RFU** 0 = Must be programmed to 0 1 = Reserved
1:0	**RFU** 0 = Must be programmed to 0 1 = Reserved

Notes: 1. Not allowed when 1/4 rate gear-down mode is enabled.

CAS WRITE Latency

CAS WRITE latency (CWL) is defined by MR2[5:3] as shown in the MR2 Register Definition table. CWL is the delay, in clock cycles, between the internal WRITE command and the availability of the first bit of input data. The device does not support any half-clock latencies. The overall WRITE latency (WL) is defined as additive latency (AL) + parity latency (PL) + CAS WRITE latency (CWL): WL = AL +PL + CWL.

Low-Power Auto Self Refresh

Low-power auto self refresh (LPASR) is supported in the device. Applications requiring SELF REFRESH operation over different temperature ranges can use this feature to optimize the I_{DD6} current for a given temperature range as specified in the MR2 Register Definition table.

CA Parity Persistent Error Mode

Normal CA parity mode (CA parity persistent mode disabled) no longer performs CA parity checking while the parity error status bit remains set at 1. However, with CA parity persistent mode enabled, CA parity checking continues to be performed when the parity error status bit is set to a 1.

ODT Input Buffer for Power-Down

This feature determines whether the ODT input buffer is on or off during power-down. If the input buffer is configured to be on (enabled during power-down), the ODT input signal must be at a valid logic level. If the input buffer is configured to be off (disabled during power-down), the ODT input signal may be floating and the device does not provide $R_{TT(NOM)}$ termination. However, the device may provide $R_{TT(Park)}$ termination depending on the MR settings. This is primarily for additional power savings.

CA Parity Error Status

The device will set the error status bit to 1 upon detecting a parity error. The parity error status bit remains set at 1 until the device controller clears it explicitly using an MRS command.

CRC Error Status

The device will set the error status bit to 1 upon detecting a CRC error. The CRC error status bit remains set at 1 until the device controller clears it explicitly using an MRS command.

CA Parity Latency Mode

CA parity is enabled when a latency value, dependent on ^{t}CK, is programmed; this accounts for parity calculation delay internal to the device. The normal state of CA parity is to be disabled. If CA parity is enabled, the device must ensure there are no parity errors before executing the command. CA parity signal (PAR) covers ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, and the address bus including bank address and bank group bits. The control signals CKE, ODT, and CS_n are not included in the parity calculation.

For the x8 configuration, the same pattern is repeated on the lower nibble as on the upper nibble. READs to other MPR data pattern locations follow the same format as the x4 case. A read example to MPR0 for x8 and x16 configurations is shown below.

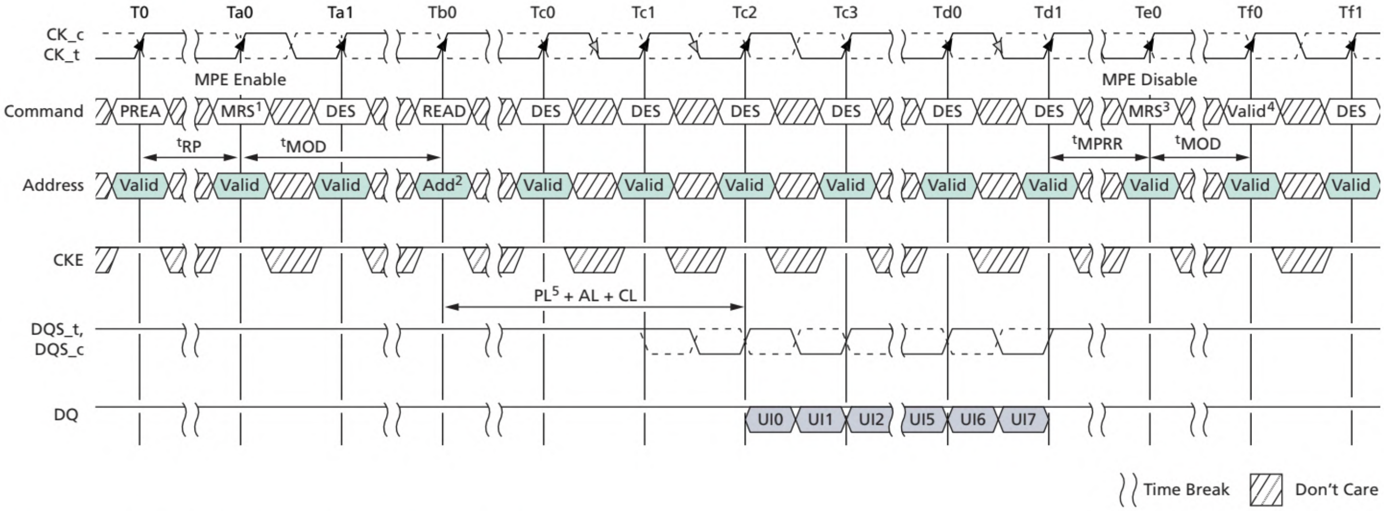
Table 35: MPR Readout Staggered Format, x8 and x16

x8 READ MPR0 Command		x16 READ MPR0 Command		x16 READ MPR0 Command	
Stagger	**UI[7:0]**	**Stagger**	**UI[7:0]**	**Stagger**	**UI[7:0]**
DQ0	MPR0	DQ0	MPR0	DQ8	MPR0
DQ1	MPR1	DQ1	MPR1	DQ9	MPR1
DQ2	MPR2	DQ2	MPR2	DQ10	MPR2
DQ3	MPR3	DQ3	MPR3	DQ11	MPR3
DQ4	MPR0	DQ4	MPR0	DQ12	MPR0
DQ5	MPR1	DQ5	MPR1	DQ13	MPR1
DQ6	MPR2	DQ6	MPR2	DQ14	MPR2
DQ7	MPR3	DQ7	MPR3	DQ15	MPR3

MPR READ Waveforms

The following waveforms show MPR read accesses.

Figure 36: MPR READ Timing



Notes: 1. $^{t}CCD\_S = 4^{t}CK$, Read Preamble = $1^{t}CK$.
2. Address setting:
A[1:0] = 00b (data burst order is fixed starting at nibble, always 00b here)
A2 = 0b (for BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7)
BA1 and BA0 indicate the MPR location
A10 and other address pins are "Don't Care," including BG1 and BG0. A12 is "Don't Care" when MR0 A[1:0] = 00 or 10 and must be 1b when MR0 A[1:0] = 01
3. Multipurpose registers read/write disable (MR3 A2 = 0).
4. Continue with regular DRAM command.
5. Parity latency (PL) is added to data output delay when CA parity latency mode is enabled.